v3.2 STUDY: QSOP24 / W→E and S→N UART / I2C recovery / LED_BLANK high = OFF

v3.2: external regulated 3.3V +/−5% only.
Single33R0805 per row; existing LED pulse/current limits retained.
R11/R12: FIT one pair per entire I2C array; DNP elsewhere.
J1 EAST TX; J3 WEST RX; J4 NORTH TX; J5 SOUTH RX.
Opposite-edge pad numbers align only with every tile upright.
J2: 1 REF, 2 SWIO/PD1, 3 GND. PC5 remains RESET.
PC4 LED_BLANK high = all columns off; keep high during reset/update.
Initial SWIO provisioning required for custom I2C recovery loader.
49.6mm square / 6.2mm pixel and edge pitch. UNROUTED STUDY.
Same-supply array only; hot-plug and physical operation unqualified.

CH32V006EBR6; W→E and S→N UART; shared I2C; no routing

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